

features of the claimed invention. Therefore, the claims as amended particularly point out and distinctly claim a subject matter which the Applicant regards as the invention. Accordingly, reconsideration and withdrawal of the indefiniteness rejection of claims 8-21 are requested.

II. Claims Rejected Under 35 U.S.C. §103

Claims 8-13 and 15-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,963,810 issued to Gardner, et al. (hereinafter “Gardner”) in view of U.S. Patent No. 4,015,281 issued to Nagata, et al. (hereinafter “Nagata”), and U.S. Patent No. 5,990,516 issued to Momose, et al. (hereinafter “Momose”).

In order to establish a *prima facie* case of obviousness, the Examiner must show that the cited references combined teach or suggest every element of the claim. In regard to claims 8 and 15, the Examiner states that “[t]he dielectric layers are inherently capable of being scaled because they have the same structure and materials as the claimed invention.” (Office Action page 3) However, Gardner teaches away from scalability in the range claimed teaching a thickness range from about 100-3,000 angstroms for a gate insulating layer. This range is well outside the stack thickness necessary to scale for feature size technology with a gate length between 25-150 nm. Therefore, Gardner does not teach a first and second dielectric material being scalable for feature size technology having a gate length in the range of 25-150 nm. Neither Nagata nor Momose cure this defect in Gardner. Momose discloses only a single gate dielectric layer. Momose’s teachings are also limited to gates of lengths less than 0.3 micrometers and to gate insulating films of less than 2.5 nm. See Momose, col. 2, lines 52-58. Thus, Momose does not teach a first and second dielectric material that can be scaled for feature size technology having a gate length in the range of 25-150 nm. Nagata does not teach any relationship between dielectric layers in terms of their dielectric constants. Nagata teaches only varying the thickness of two dielectric layers so that either may predominate over the other to selectively induce electrons or holes in the surface of the substrate. Nagata, col. 2, lines 46-64. Therefore, nothing in the cited references of Gardner, Nagata or Momose teaches or suggests a first and second dielectric material being scalable for

feature size technology having a gate length in the range of 25-150 nm. Accordingly, reconsideration and withdrawal of the rejection of claims 8 and 15 are requested.

In regard to claims 9 and 16, Gardner does not specify a dielectric constant for the nitride layer with a high permitivity layer. Thus, Gardner cannot be said to disclose a second dielectric layer having a greater dielectric constant from the first dielectric material. Neither Nagata or Momose teaches a second dielectric layer having a dielectric constant greater than the first as discussed in regard to claims 8 and 15, above. Further, claims 9 and 16 incorporate the limitation of claims 8 and 15, respectively, and are not obvious at least for the reasons mentioned in regard to claims 8 and 15. Accordingly, reconsideration and withdrawal of the rejection of claims 9 and 16 are requested.

In regard to claims 12 and 19, Applicant has reviewed the cited references and has been unable to discern any segment which teaches or suggests the first gate dielectric material being selected from one of HfO₂ or ZrO₂. Thus, Applicant requests that the Examiner indicate where in the cited references a dielectric material being selected from one of HfO₂ or ZrO₂ is taught or suggested. Accordingly, reconsideration and withdrawal of the rejection of claims 12 and 19 are requested.

In regard to claims 10, 11 and 13, these claims depend from independent claim 8 and incorporate the limitations thereof. Thus, these claims are not obvious at least for the reasons given in regard to independent claim 8. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 10, 11 and 13 are requested.

In regard to claims 17, 18 and 20, these claims depend from independent claim 15 and incorporate the limitations thereof. These claims therefore are not obvious at least for the reasons given in regard to independent claim 15. Accordingly, reconsideration and withdrawal of the rejection of claims 17, 18 and 20 are requested.

Claims 14 and 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of Nagata and Momose, and in further view of U.S. Patent No. 5,258,645 issued to Sato (hereinafter “Sato”). Applicant respectfully disagrees for the following reasons.

Claims 14 and 21 depend from claims 8 and 15 respectively, and thus incorporate the limitations of those claims. Therefore claims 14 and 21 are not obvious over Gardner, Nagata and Momose, at least for the reasons given in regard to claims 8 and 15. Applicant has reviewed Sato and has been unable to discern any portion of Sato that teaches or suggests a first and second dielectric material being scalable for feature size technology having a gate length in the range 25-150 nm. Accordingly, reconsideration and withdrawal of the rejection of claims 14 and 21 are requested.

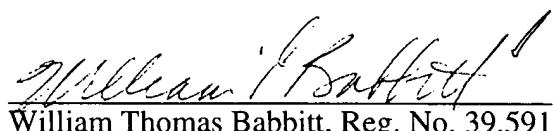
CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 8-21 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action as earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the Application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

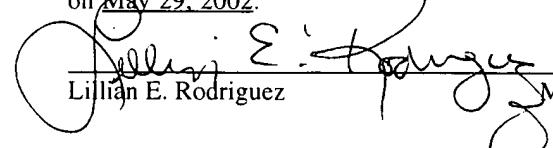
Dated: May 29, 2002


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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited as First Class Mail with the United States Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Box Non-Fee Amendment, Washington, D.C. 20231 on May 29, 2002.


Lillian E. Rodriguez

May 29, 2002

5-29-02

VERSION WITH MARKINGS TO SHOW CHANGES MADE ✓

IN THE CLAIMS

8. (Four Times Amended) A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:

- a first dielectric material having a first dielectric constant;
- a second dielectric material having a second dielectric constant different from the first dielectric constant; and

the first and second dielectric materials being scalable for a feature size technology having a gate length in the range of 25-150nm.

15. (Three Times Amended) An apparatus comprising:

a semiconductor substrate having a transistor device formed thereon, the transistor device having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising:

- a first dielectric material having a first dielectric constant;
- a second dielectric material having a second dielectric constant different from the first dielectric constant; and

the first and second dielectric materials being scalable for a feature size technology having a gate length in the range of 25-150nm.